2016

Question 2: Short Questions

a) Press M-N using r's compliment when M = 2750 and N = 750 are in decmal number system.

Answer:

M-N means

$$\begin{array}{r} 2750 \\ -\ 750 \\ \hline 2000 \end{array}$$

As base is 10 for decmal number system so r's compliment will be 10's compliment

2750 —(1)

750 —(11)

Take 10's compliment of (11)

$$\begin{array}{r} 9999 \\ -\ 750 \\ \hline 9249 \\ +\ 1 \\ \hline 9250 \end{array}$$ —(111)

Add (1) and (111)

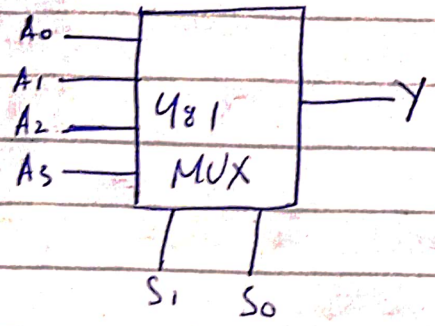
$$\begin{array}{r} 2750 \\ +\ 9250 \\ \hline 12000 \end{array}$$

carry drop ← 12000 Ans

b) Design 4:1 Multiplexer.

Answer To construct a 4:1 MUX, we need 2 selection lines let suppose S_0 and S_1.

S_0,



It will select one input from the input lines according to selection lines data.

c) Express the given functions in a sum of minterms and a product of maxterms.

Answer

$$F(A,B,C,D) = D(A' + B) + B'D$$

$$F(A,B,C,D) = A'D + BD + B'D \quad \text{for SOP}$$

POS is a compliment of SOP, so

$$\overline{F(A,B,C,D)} = \overline{(A'D) + (BD) + (B'D)}$$

$$= \overline{(A'D)} \cdot \overline{(BD)} \cdot \overline{(B'D)}$$

$$= (\bar{A} + \bar{D}) \cdot (\bar{B} + \bar{D}) \cdot (\bar{B} + \bar{D})$$

$$= (A + \bar{D}) \cdot (\bar{B} + \bar{D}) \cdot (B + \bar{D}) \quad \text{Ans}$$

d) Draw the truth table of Half Adder circuit?

Answer

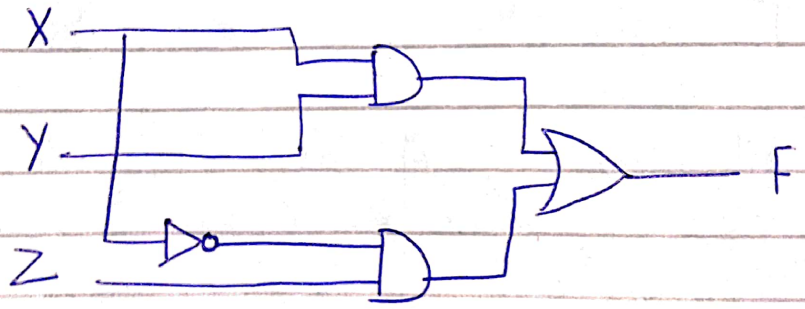
Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

e) Draw a circuit for given function using NAND gate only.

$$F(X, Y, Z) = XY + X'Z$$

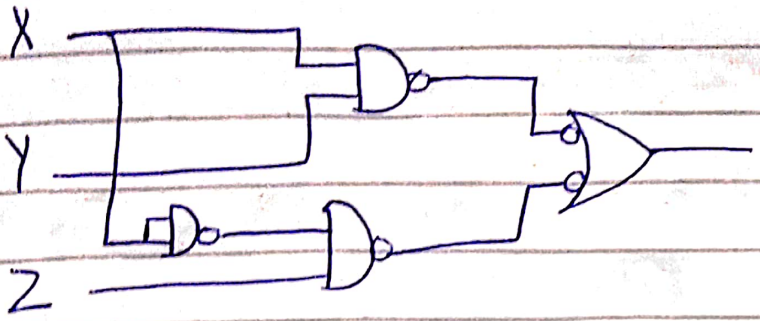
Answer:

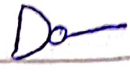
First draw the circuit,

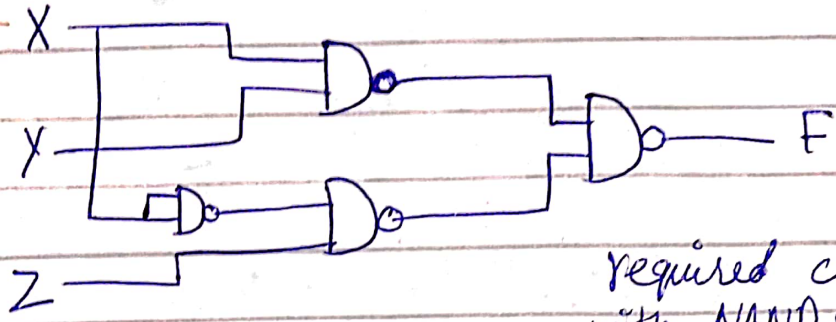


Add (0) inverter on inputs of OR gate and output of AND gates and replace NOT gate with ( ) to ( )

So,



Replace  with 



required circuit with NAND gates only

f) What is the difference between ROM and RAM?

Answers

RAM	ROM
→ Stands for Random Access Memory	→ Stands for Read Only Memory.
→ It is a volatile memory.	→ It is a non-volatile memory.
→ Can do both read and write operations	→ Can do only read operations.
→ memory capacity is upto 256 gb per chip.	→ memory capacity is upto 4 to 8 MB per chip.
→ The data stored in RAM is lost in case of power failure.	→ The data in ROM doesn't lose in case of power failure

g) Give the excitation table for JK flipflop.

Answer

Excitation Table is:

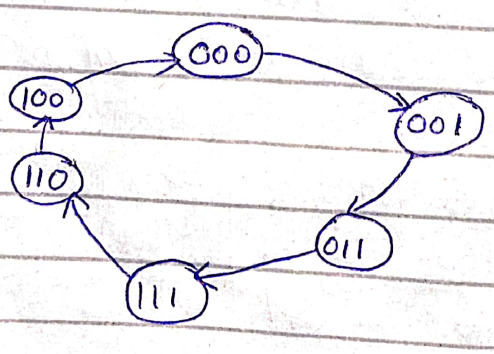
Present State Qn	Next State Qn+1	Inputs J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Question 3: Long Questions

a) Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use JK-FlipFlops.

Answer

3-bit Synchronous counter will be used for this sequence with the help of JK FlipFlops. 3-bits means 3 FlipFlops will be used.



Transition Tables:

Present State			Next State			Inputs			
Q_2	Q_1	Q_0	Q_2'	Q_1'	Q_0'	J_2 K_2	J_1 K_1	J_0 K_0
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	1	0 X	1 X	X 0
0	1	1	1	1	1	1 X	X 0	X 0
1	1	1	1	1	0	X 0	X 0	X 1
1	1	0	1	0	0	X 0	X 1	0 X
1	0	0	0	0	0	X 1	0 X	0 X

Now, we have to find the values of J_2, J_1, J_0 and K_2, K_1, K_0 in terms of Q_2, Q_1, Q_0 using K-maps:

J_2

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	0	X	X

$J_2 = Q_1Q_0$

K_2

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	0
1	1	0	0	0

$K_2 = Q_1'Q_0'$

J_1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	
1			X	X

$J_1 = Q_1Q_0$

K_1

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X		
1	X			1

$K_1 = Q_2Q_0'$

J_1

Q_2 \ Q_1Q_0	00	01	11	10
0		1	X	
1			X	X

$J_1 = Q_2' Q_0$

J_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	
1			X	

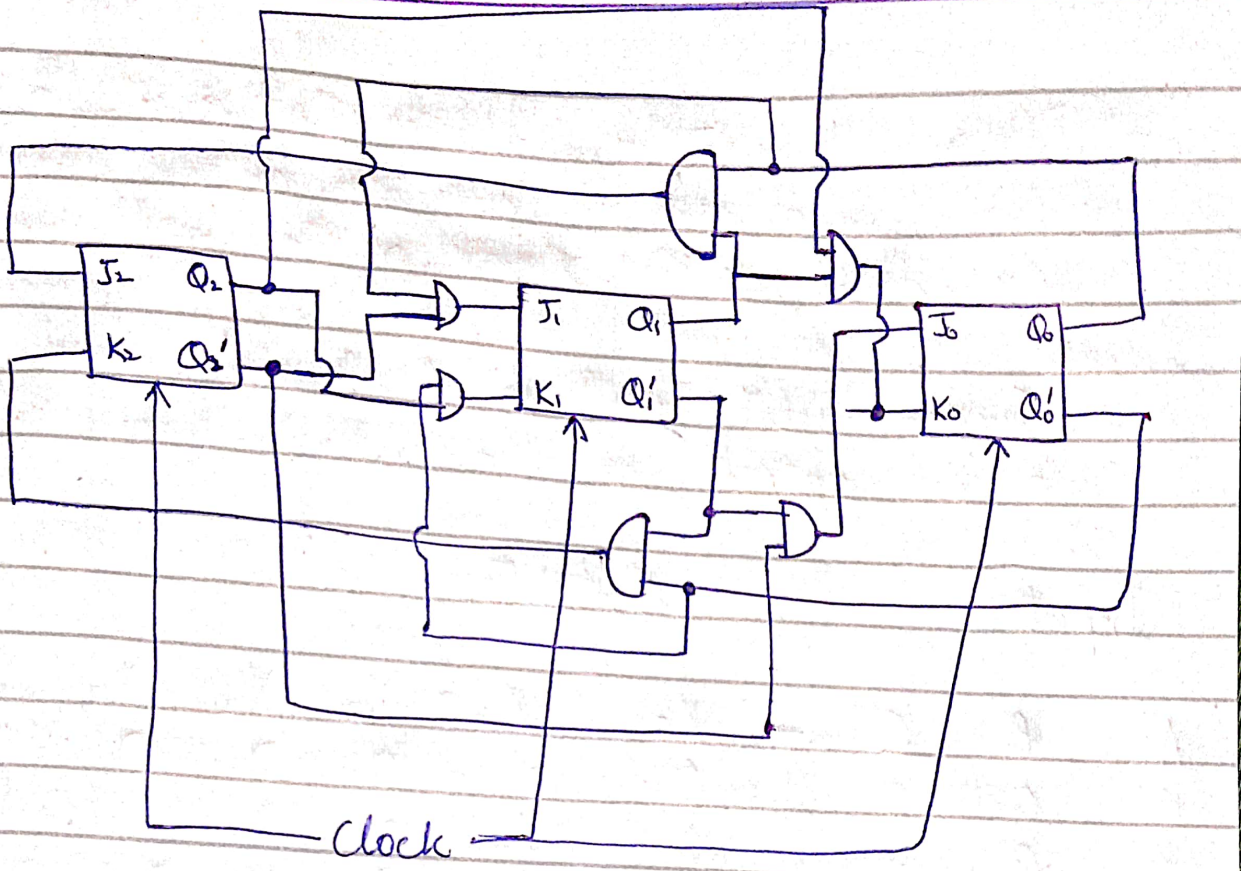
$J_0 = Q_2' Q_1'$

K_0

Q_2 \ Q_1Q_0	00	01	11	10
0	X			
1	X		1	X

$K_0 = Q_2 Q_1$

Circuit Diagram:


J2
Q2
K2
Q2'
J1
Q1
K1
Q1'
J0
Q0
K0
Q0'
Clock

b) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.

Answers

Suppose 3-bit input as A, B and C and 6-bit output as X_5, X_4, X_3, X_2, X_1 and X_0.

Inputs			Outputs					
A	B	C	X_5	X_4	X_3	X_2	X_1	X_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$X_5 = ABC' + ABC = AB(C + C') = AB$

$X_4 = ABC + AB'C + AB'C' = ABC + AB'(C + C')$
$= ABC + AB' = A(BC + B') = A(B + B')(B' + C)$
$= A(B' + C) = AB' + AC$

$X_3 = A'BC + AB'C = C(A'B + AB') = C(A \oplus B)$

$X_2 = A'BC' + ABC' = BC'(A' + A) = BC'$

$X_1 = 0$

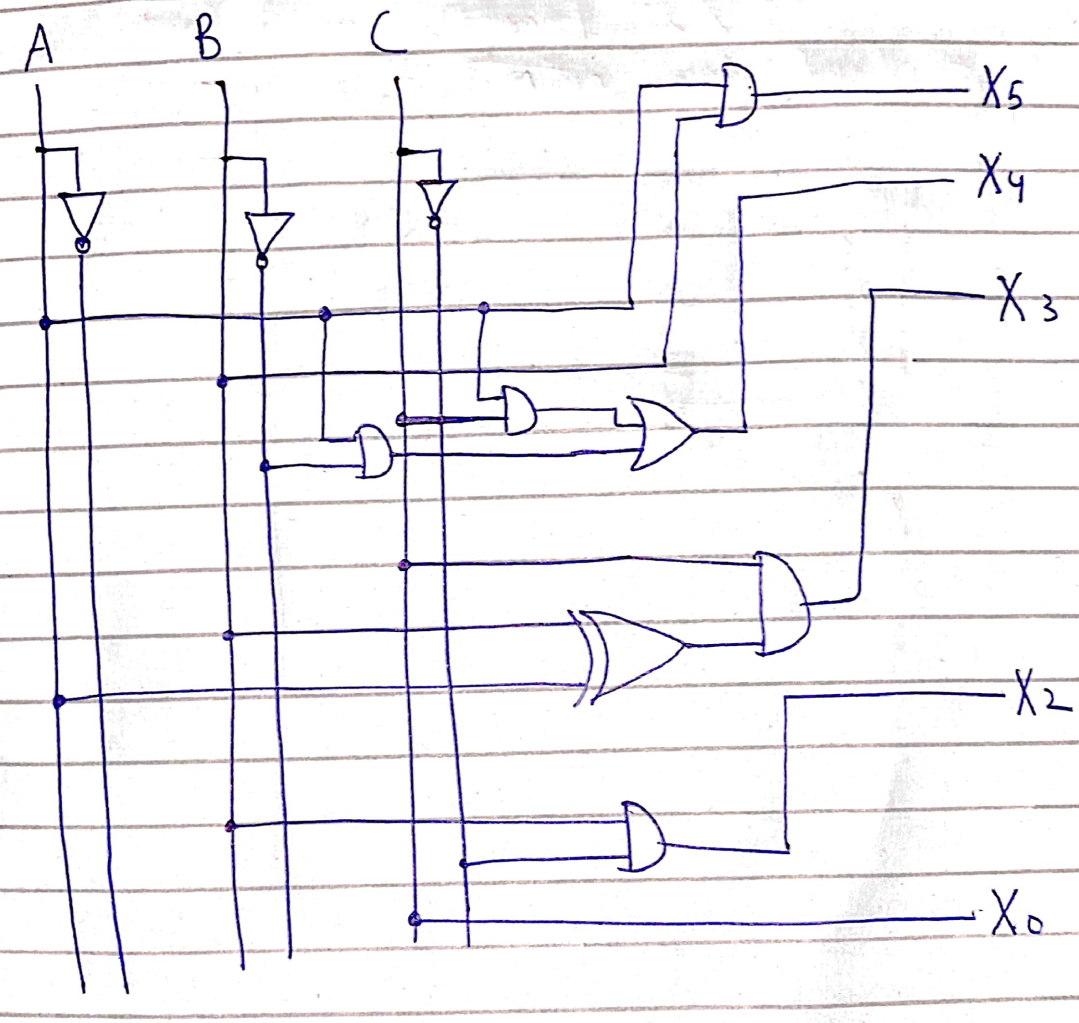
$X_0 = A'B'C + A'BC + AB'C + ABC$

$= A'C(B'+B) + AC(B'+B)$

$= A'C + AC = C(A'+A)$

$X_0 = C$

Circuit Diagram:



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Full Subtractor

3 inputs 2 outputs : difference, borrow

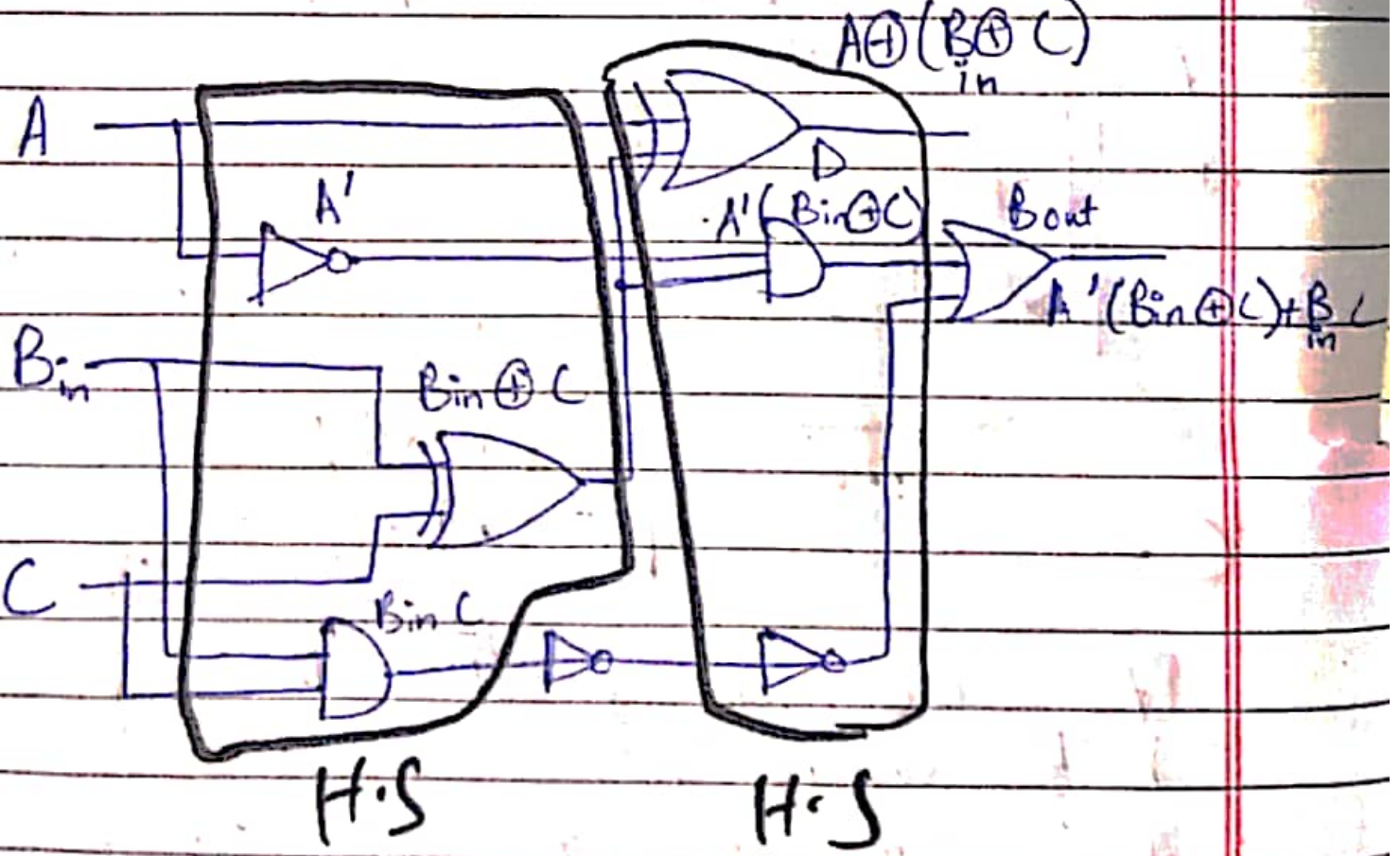
3 Inputs = 2^3 = 8 combinations

X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$= \bar{X}(\bar{Y}Z + Y\bar{Z}) + X(\bar{Y}\bar{Z} + YZ)$$
$$= \bar{X}(Y \oplus Z) + X(Y \odot Z)$$
$$= \bar{X}(Y \oplus Z) + X(\overline{Y \oplus Z})$$
$$= X \oplus (Y \oplus Z)$$

$$B = X'Y'Z + X'YZ' + X'YZ + XYZ$$
$$= X'(Y'Z + YZ') + YZ(X + X')$$
$$= X'(Y \oplus Z) + YZ$$

Full Subtractor with Two Half Subtractors:



c) ii) Draw 4 X 2 Encoder circuit.

Answer:

Encoder is a combinational circuit having 2^n input lines and n output lines

$$2^n \times n$$

So, 4 X 2 Encoder will have four inputs and two outputs.